Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor memory system comprising:

a memory controller;

N system data buses connected to the memory controller, each of the *N* system data buses having a width of *M/N* bits, where *M* is a natural number and *N* is a natural number greater than or equal to 2; and

first through *P*-th memory module groups, each of the first through *P*-th memory module groups having *N* memory modules, where *P* is a natural number greater than or equal to 2;

wherein the *N* memory modules within each of the first through *P*-th memory module groups are respectively connected to the *N* system data buses;

wherein the first through *P*-th memory module groups are operated in response to respective first through *P*-th chip select signals; and,

wherein the *N* system data buses are wired such that data transmission times between the *N* memory modules within each of the first through *P*-th module groups and the memory controller are the same.

2. (Original) The system of claim 1, wherein *M* is a bit-width of an entire system data bus of the semiconductor memory system.

3. (Canceled)

4. (Previously Presented) The system of claim 1, wherein each of the *N* memory modules includes *L* memory devices divided into two or more banks; and,

wherein the two or more banks within each of the N memory modules share a data bus of *M/N* bits and the two or more banks within each of the N memory modules are separately operated in response to two or more corresponding chip select signals.

5. (Previously Presented) The system of claim 4, wherein the two or more banks within each of the N memory modules respectively receive the two or more corresponding chip select signals.

6. (Original) The system of claim 4, wherein each of the *L* memory devices has a data bus width of *M/L* bits.

7. (Original) The system of claim 1, wherein each of the *N* memory modules includes *L* memory devices, and wherein each of the *L* memory devices has a bus width of *M/(N*L)* bits.

8. (Previously Presented) A semiconductor memory system comprising:

a memory controller;

N system data buses connected to the memory controller, each of the *N* system data buses having a width of *M/N* bits, where *M* is a natural number and *N* is a natural number greater than or equal to 2;

a first memory module group having *N* memory modules respectively connected to the *N* system data buses, wherein the *N* memory modules of the first memory module group each have a data bus width of *M/N* bits and are operated in response to first chip select signals; and

a second memory module group having at least one memory module connected to all of the *N* system data buses, wherein the at least one memory module of the second memory module group has a data bus width of M bits and is operated in response to a second chip select signal; and,

wherein the *N* system data buses are wired such that data transmission times between each of the memory modules in the first memory module group and the memory controller are the same.

9. (Original) The system of claim 8, wherein *M* is a bit-width of an entire system data bus of the semiconductor memory system.

10. (Canceled)

11. (Previously Presented) The system of claim 8, wherein each of the memory modules of the first memory module group includes *L* memory devices divided into two or more banks, wherein the two or more banks share a data bus of *M/N* bits and are separately operated in response to the first chip select signals.

12. (Previously Presented) The system of claim 11, wherein the first chip select signals are respectively applied to the two or more banks.

13. (Original) The system of claim 11, wherein each of the *L* memory devices has a data bus width of *M/L* bits.

14. (Original) The system of claim 8, wherein each of the memory modules includes *L* memory devices, and each of the *L* memory devices has a bus width of *M/(N*L)* bits.

15. (Currently Amended) A semiconductor memory system, the system comprising:

a memory controller;

N system data buses connected to the memory controller, each of the *N* system data buses including a plurality of data buffers and having a width of *M/N* bits, where *M* is a natural number and *N* is a natural number greater than or equal to 2; and

first through *P*-th memory module groups connected to the *N* system data buses, each of the first through *P*-th memory module groups having *N* memory modules, wherein P is a natural number greater than or equal to 2;

wherein the *N* memory modules within each of the first through *P*-th memory module groups are respectively connected to the data buffers of the *N* system data buses;

wherein the first through *P*-th memory module groups are operated in response to respective first through *P*-th chip select signals; and,

wherein the *N* system data buses are wired such that data transmission times between the *N* memory modules within each of the first through *P*-th module groups and the memory controller are the same.

16. (Original) The system of claim 15, wherein *M* is a bit-width of an entire system data bus of the semiconductor memory system.

17. (Canceled)

18. (Previously Presented) The system of claim 15, wherein each of the memory modules of the first memory module group includes *L* memory devices;

wherein the *L* memory devices are divided into two or more banks; and,

wherein the two or more banks of each of the *L* memory devices share a data bus of *M/N* bits and are separately operated in response to two or more corresponding chip select signals.

19. (Previously Presented) The system of claim 18, wherein the two or more banks of each of the *L* memory devices respectively receive the two or more corresponding chip select signals.

20. (Original) The system of claim 18, wherein each of the *L* memory devices has a data bus width of *M/L* bits.

21. (Original) The system of claim 15, wherein each of the memory modules includes *L* memory devices, and each of the *L* memory devices has a bus width of *M/(N*L)* bits.

22. (Previously Presented) The system of claim 4, wherein each of the *L* memory devices in each of the *N* memory modules shares a data pin with at least one other memory device.

23. (Previously Presented) The system of claim 1, further comprising:
first through P-th data buffers connected to each of the *N* system data buses.

24. (Previously Presented) The system of claim 11 wherein each of the *L* memory devices in each of the *N* memory modules shares a data pin with at least one other memory device.

25. (Previously Presented) The system of claim 8, further comprising:
first through P-th data buffers connected to each of the *N* system data buses.